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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,802	12/22/2000	Michihide Kimura	1448.1007	9060

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,802	KIMURA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,13-18,20-22 and 24-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-22 and 24-28* is/are allowed.

6)☒ Claim(s) *14,16 and 18* is/are rejected.

7)☐ Claim(s) *13,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/22/00* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/28/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claims 2-6, 13-18, 20-22,24-28 remain for examination. Claims 1,7-12,19,23, 29-32 have been canceled.

1. Applicant's arguments with respect to claims 13,14,17 have been considered but are moot in view of the new ground(s) of rejection.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 14,16,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett (6,167,479) in view of Yamahata (4,847,748).

2. As to newly amended claim 14, Hartnett also taught at least :

a) exception processing method for a processor that executes a program including a first instruction and a second instruction, and that performs, after an interruption caused by the second instruction and before execution of interrupt processing, exception processing for an exception that has occurred during execution of the first instruction, wherein the first instruction is a specific application-purpose operation instruction (see special purpose instruction in col.7, lines 41-65), the execution comprising :

1) setting when the exception occurs during the execution of the first instruction, a value indicating occurrence of the exception in interrupt signals (see detection of fault and non-fault events in col.10, lines 1-34) ;

2) determining when the interruption was caused by the second instruction, whether the exception has occurred by reading the interrupt signals (see , the state of reflecting the fault and non-fault interrupts, see also determination of what caused interrupt in col.11, lines 5-37, col.12, lines 5-8);

3) performing the exception processing for the first instruction, if the exception has occurred according to interrupt signals (see interrupt handler in col.12, lines 5-51): and;

4) performing the interrupt processing for the second instruction to return from the interruption see return instruction in col.15, lines 44-56, col.17, lines 1-40).

3. Hartnett did not specifically show his exception signals were set in register or flag as clamed. However, Yamahata disclosed a system for setting exception flag in a queue (see col.8, lines 47-52). It would have been obvious to one of ordinary skill in the art to use Yamahata in Hartnett for including the setting of the register or the flag indicating the exception as claimed because the use of Yamahata could provide Hartnett the ability to identify the exceptions occurred at predefined set of processing points, and it could be achieved by configuring the exception flag of Yamahata in Harnett so that the specific exception flag of Yamahata could be recognized by Hartnett in order to resume at the interrupt detection, and because Hartnett did disclosed a confirmation of an exception (see the interrupt type in col.10! lines 51-53,

see also the state reflecting the fault and non-fault type interrupt in col.11 , lines 5-37, see also determination of what caused the interrupt in col.12, lines 5-8, the specific application – purpose instruction was already taught in 7, lines 41-65), which was a suggestion of the need for setting the exception in register or a flag in order to resume the execution path , and in doing so, provided a motivation.

4. As to claim 16, also determine the predetermined instruction (see fault and no-fault type of instruction in col.).

5. As to claim 18, Hartnett also included instruction address in a table .

6. Claims 13, 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior ad of record further teaches the detailed functions of the determination before the execution of the exception processing whether to perform the exception by reading the second register a or a second flag that store operating mode indicating the processor whether to perform the exception.

7. Claims 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior ad of record further teaches the detailed functions of the determining before the execute-on of the

execution processing, whether to perform the exception processing by checking whether a value which is stored in a second register or a second flag, and is associated with the second instruction that has caused the exception indicates the processor to perform the exception processing.

8. Claims 20-22 are allowable over the ad of record '. None of the prior art or record teaches combined features of :

a) the exception detection flags, the specific application purpose instruction execution setting the valid operation exception sate , notification of the interrupt control due to the of instruction when the flag was set to valid state during the trap to generate the interruption and the exception detection flag invalidating instruction and invalidation the exception detection flag (claim 20),

b) the exception detection flags, the specific application purpose instruction execution setting the valid sate , notification of the interrupt control due to the operation exception of the instruction when the flag was set to valid state during the trap to generate the interruption and the excepti6n detection flag read instruction (claim 21) '

c) the execution setting the valid sate , notification of the interrupt control due to the exception detection flags, the specific application purpose instruction operation exception of the instruction when the flag was set to valid state during the trap to generate the interruption and the exception detection flag write instruction (claim 22) .

9. Claims 24-28 are allowable over the art of record for reciting the combined features of the condition code register and the branch/interrupt return instruction control unit for determining the interrupt generation based on the value held in the condition code register and .the value in the instruction field during the execution of the trap instruction, and the notification that the interrupt is to be generated.

Applicant's amendment (to claim 14) necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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